

Design of MAC Unit for Complex Numbers in VHDL

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ABSTRACT: In Digital Communication, Digital Signal Processor (DSP) is an important block which performs several digital signal processing applications such as Convolution, Discrete Cosine Transform (DCT), Fourier Transform, and so on. Every digital signal processor contains MAC unit. The MAC unit performs multiplication and accumulation processes repeatedly in order to perform continuous and complex operations in digital signal processing. In this paper 16-bit MAC unit is designed and implemented. The multiplier used are Wallace Tree multiplier and Baugh Wooley multiplier. The total design program is synthesis and simulated on Xilinx software and the parameter results of the pipelined Baugh Wooley multiplier is found to be better than that of Wallace Tree multiplier.

I. INTRODUCTION

With the increasing popularity of the smart phones and TABs, speed of the processor has become so important nowadays. Though the need for the processor's speed is more exploited for gaming and multimedia application purposes, it can also be deployed in fields like medical for faster diagnosis, in automation industry for higher throughput and so on. Since most of the signal processing operations is done by adders and multipliers units, efficient design of these units increases the speed of the processor. MAC unit is mainly used in several multimedia applications, careful design of this MAC unit leads to the design of high performance processor. The speed of the conventional MAC unit is optimized by using various frontline multipliers like Wallace tree multiplier, Booth Multiplier, Baugh-Wooley multiplier.

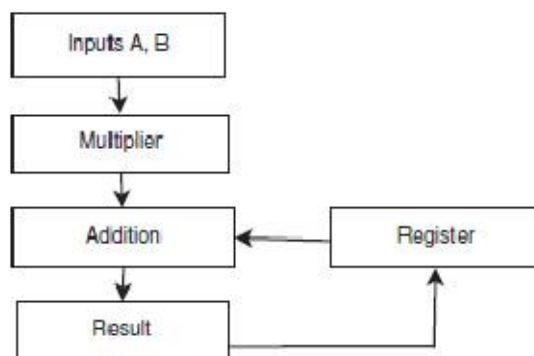


Fig 1: Block Diagram of MAC

In general, digital signal processors are used to perform the digital signal processing operations like convolution, correlation, transform and filtering. All the above mentioned digital signal processing operations are in the form of multiplication and repeated addition. So multiply accumulate circuit (MAC) is the heart of the digital signal processor. The signal sequences can be represented as fixed/floating point complex numbers. Complex numbers are playing a vital role in electronics and digital signal processing (DSP), because they are easy way to represent and manipulate the most useful real world sinusoidal waveforms. The signal attributes like amplitude and phase, can be revealed easily by complex numbers than real numbers. The basic blocks of MAC is shown in Fig. 1, where the inputs A and B are

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multiplied then the multiplication result is added with the previous MAC result. If A, B are n bits wide then the multiplication result will be 2n bits wide. So to avoid overflow during accumulation, the accumulation register will have k extra bits with its actual length of 2n bits. The multiplier is the part of the MAC which can be designed in many ways. Array multiplier and Wallace tree multiplier are the popular multipliers that are used in hardware implementation. The array multiplier can be further classified into two categories namely, ripple carry array multiplier and carry save array multiplier. The carry save array multiplier can be designed in many ways, they are Braun Multiplier and Baugh Wooley multiplier. The second part of the MAC is accumulator which can be designed in several ways namely, ripple carry adder and carry look ahead adder.

II. LITERATURE REVIEW

In the paper [1], a high performance 32-bit radix-2 fixed point complex number MAC is proposed, where the real and imaginary parts can be computed by sending the previous MAC result as one of the partial product to the present multiplication. So the depth of the MAC is equal to the depth of the multiplier. And hence the separate accumulator circuit is avoided. The experimental results are showing the proposed fixed point complex number MAC is giving better performance than the conventional fixed point complex number MAC. The proposed architecture achieves an improvement factor of 32.4% in Wallace tree and 19.1% in Braun multiplier based fixed point complex number MAC without pipeline using 45 nm technology library. The same architecture achieves an improvement factor of 14.6% in Wallace tree and 12.2% in Braun multiplier based fixed point complex number MAC with pipeline. In paper [2], fixed-width modified Baugh Wooley multiplier has been realized using Virtex-7, Artix-7 and Zynq- 7000 FPGAs. The design has been coded in VHDL using modular approach. The performance of the multiplier is evaluated based on area, speed and power using different design optimization goals such as balanced, area reduction, timing performance and power optimization. Optimal results are obtained with balanced approach as compared to other techniques. As a future work, a generic reconfigurable power efficient and low-error fixed-width Baugh-Wooley multiplier will be realized in FPGA and its performance will be analyzed and compared with other multiplier architectures. Where as in paper [3], an optimized co-processor unit, designed specifically for executing the DSP application is proposed. It can be used as a co-processor for the ACORN ARM processor. The co-processor comprises of one MAC unit, control unit, a 32 bit output registers and register files for storing the input values and other co-efficient. The co-processor is designed to execute a FIR filter. Vedic multiplier and booth multiplier has been used in the MAC unit and comparison is done based on the power, speed and area. While in paper [4], they propose a low power pipelined MAC architecture that incorporates a 16x16 multiplier using Baugh-Wooley algorithm with high performance multiplier tree, together with clock gating the idle pipeline stages to reduce the power consumption. By using the technique of clock gating independent pipeline stages of MAC architecture, we have shown that the power dissipation of the proposed MAC architecture is less than existing low power MAC units with the same performance. Simulations show that the power consumption of the proposed architecture is 30% to 80% less than the other contemporary MAC architectures, without compromising its computation performance. In paper [5], MAC unit model is designed by incorporating the various multipliers such as Array Multiplier, Ripple Carry Array Multiplier with Row Bypassing Technique, Wallace Tree Multiplier and DADDA Multiplier [6] [7] in the multiplier module and the performance of MAC unit models is analyzed in terms of area, delay and power. The performance analysis of MAC unit models is done by designing the models in Verilog HDL. Then, MAC unit models are simulated and synthesized in Xilinx ISE 13.2 for Virtex-6 family 40nm technology. Further, this work can be extended by designing of MAC unit with higher number of bit sizes such as 16, 32 and 64 and also for designing applications like ALU, filters etc.

Remarkable observations in the literature survey are Vedic, Wallace, Dadda are all unsigned multipliers, Baugh Wooley is signed multiplier and Baugh Wooley multiplier is preferred because it offers better sign bit management, uniform VLSI structure and no complex encoding circuits that results in compact circuit. The biggest advantage of compact and uniform structure is implementation of pipelining that easily divides the partial product generation stages and increases speed of operation [8] [9]

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III. PROPOSED ARCHITECTURE OF FIXED POINT COMPLEX MULTIPLIER

In digital signal processing, digital signals can be represented as amplitude and phase, which can be written as a complex number. The two complex number can be represented as $(P + jQ)$, and $(R + jS)$, where $P = \{Ps, Pm\}$, $Q = \{Qs, Qm\}$, $R = \{Rs, Rm\}$ and $S = \{Ss, Sm\}$. Herw the suffix s represent the sign bit and m represent binary number. The complex number multiplication can be done in several ways. Let real part of the multiplication of the two complex number is X and imaginary part is Y, where $X = \{Xs, Xm\}$ and $Y = \{Ys, Ym\}$. According to [1], FPCN multiplication requires two fixed point multiplication and two fixed point adder. The fixed point complex number fixed point multiplier-cum accumulators shown in Fig.2 consist of two fixed point multipliers and two fixed point adders followed by accumulator.

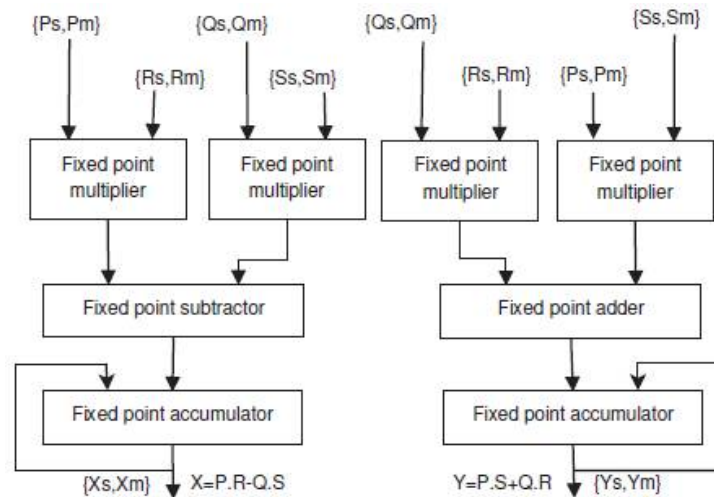


Fig 2.Fixed point complex number multiplier-cum-accumulator

1. MAC using Baugh Wooley multiplier

Baugh-Wooley Multiplier is used as a signed number multiplication. Signed Number operands which are represented in 2's complement form. Partial Products are adjusted such that negative sign move to last step, which in turn maximize the regularity of the multiplication array. Baugh-Wooley Multiplier operates on signed operands with 2's complement representation to make sure that the signs of all partial products are positive. Fig 3 shows the structure of Baugh wooley multiplier. As this structure is uniform it can be easily pipelined because of which the initial delay may increase but the operating frequency of the multiplier increases. At every stage the pipeline registers are applied so that the structure a]can operate with same clock signal. For the 16- Bit Baugh wooley multiplier, number of pipeline stages used are 18 stages.

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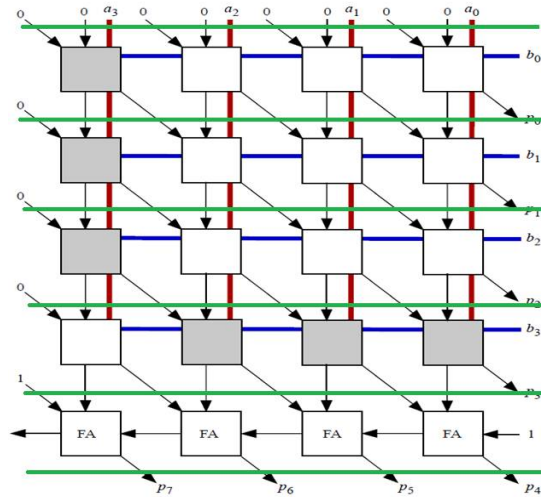


Fig 3. Pipelined Baugh Wooley Multiplier

The MAC is designed using this Fixed point complex signed Baugh wooley multiplier. The adder used after multiplier is CLA(carry look ahead adder) as it has minimum delay. The structure of MAC using pipelined Baugh wooley is such that, we don't have to separately pipeline MAC to get results.

Multiplier	No. of I/O (out of 172)	Delay	Circuit throughput (Frequency)	Power		
				Dynamic Power	Leackage Power	Total Power
16-Bit	131	5.376 ns	186.011 MHz	2.194 W	0.346 W	2.540 W

Table 1.Result if proposed MAC using 16-Bit Baugh Wooley Multiplier

2. MAC using Wallace Tree multiplier

The Fig 4. shows Wallace tree multiplier consisting of three steps. In first step, the partial products are obtained by multiplying the bits of multiplier and the multiplicand. Where as in step second by using half adder and full adder the bit product matrix is reduced to lower number of rows. In the final step of operation , the addition is done using the adder. But the Wallace tree Multiplier is a unsigned multiplier, so it cannot be used for the sign bit multiplication. The structure of Wallace multiplier is not uniform as compared with the Baugh wooley multiplier so it cannot be pipelined. As number of stages increases for larger bit the area utilization is also large.

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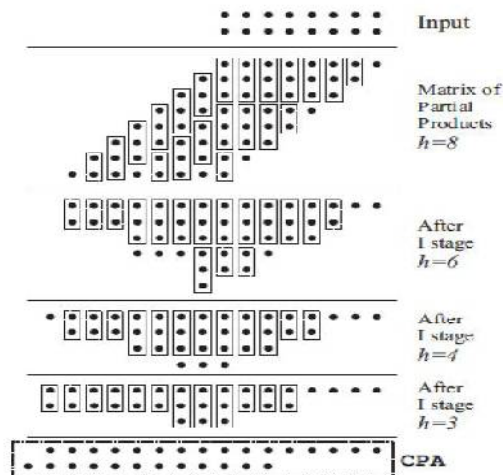


Fig 4. Wallace tree multiplier

The Fixed point complex MAC is designed using 16- Bit Wallace tree multiplier as well as carry look ahead adder and the results are compared with the fixed point complex MAC using Baugh wooley multiplier .

Multiplier	No. of I/O (out of 172)	Delay	Circuit throughput (Frequency)	Power		
				Dynamic Power	Leackage Power	Total Power
16-Bit	130	3.135 ns	319.02 MHz	3.012 W	0.357 W	3.269 W

Table 2. Result of proposed MAC using 16-Bit Wallace tree Multiplier

3. Experimental Results

The design is modeled in Verilog HDL. This Verilog HDL models are simulated and verified using Xilinx ISE simulator. The designs are implemented in Vertex-5 which is 65nm technology. The experimental results of complex MAC using Baugh Wooley multiplier is compared with the complex MAC using Wallace tree multiplier. The Baugh wooley multiplier has the delay of 5.376 ns and power utilization of 2.540 W but for the Wallace tree multiplier gives the delay of 3.135 ns and the power consumption of 3.369 W. Here the MAC designed using Baugh wooley multiplier is pipelined as well as the multiplier is a signed multiplier, but the Wallace tree multiplier is not pipelined and also it is not a signed multiplier.

4. Conclusion

In this paper, 16-bit radix-2 complex number MAC is proposed using Baugh wooley and Wallace tree multiplier. Here the real and imaginary part is calculated by sending the previous MAC result as one of the partial product to the present multiplication. So the depth of the multiplier is equal to the depth of the MAC. And hence the separate accumulator circuit is avoided. The experimental results are shows the proposed fixed point MAC using Baugh wooley multiplier gives the better performance in terms of delay, area, operating frequency and power as compared with the MAC designed using Wallace tree multiplier.

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(An ISO 3297: 2007 Certified Organization)

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REFERENCES

- [1] Mohamed Asan Basiri M, Noor Mohammad Sk, "An Efficient Hardware Based MAC Design in Digital Filters with Complex Numbers", in IEEE International Conference on Signal Processing and Integrated Networks, 2014.
- [2] Aiman Badawi, et al, "FPGA Realization and Performance Evaluation of Fixed-Width Modified Baugh-Wooley Multiplier", in IEEE International Conference on Technological Advances in Electrical, Electronics & Computer Engineering, 2015.
- [3] Rahul Narasimhan. A, R. Siva Subramanian, "High Speed Multiply-Accumulator Coprocessor Realized for Digital Filters", in IEEE International Conference on Electrical, Computer & Communication Technologies, 2015.
- [4] Rakesh Warriar, C.H. Vun, Wei Zhang, "A Low-Power Pipelined MAC Architecture using Baugh-Wooley based Multiplier", in IEEE Global Conference on Consumer Electronics, 2014.
- [5] Maroju Sai Kumar, D. Ashok Kumar, Dr. P. Samundiswary, "Design and Performance Analysis of Multiply-Accumulate (MAC) Unit", in IEEE International Conference on Circuit, Power and Computing Technologies, 2014.
- [6] Charles Roth, "Digital System Design using VHDL", in Cengage Learning, 2010.
- [7] Douglas Perry, "VHDL Programming by Examples", in Tata Mcgraw Hill, 2002.
- [8] K. Paldurai, K. Hariharan, G.C. Karthikeyan, K. Lakshmanan, "Implementation of MAC using Area Efficient and Reduced Delay Vedic Multiplier Targeted at FPGA Architectures", in IEEE International Conference on Communication and Network Technologies, 2014.
- [9] Ramandeep Kaur, Rahul Malhotra, Sujay Deb, "MAC based FIR Filter: A novel approach for Low-Power Real-Time De-noising of ECG signals", in IEEE 19th International Symposium on VLSI Design & Test, 2015.